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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,013	11/26/2001	James E. Jaussi	884.512US1	9548

7590 09/23/2003

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,013	JAUSSI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 10-20* is/are allowed.

6)☒ Claim(s) *1,7-9,21,22,24,26 and 27* is/are rejected.

7)☒ Claim(s) *2-5, 23, 25, 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in repose to the amendment filed 08/04/2003. A new ground of rejection is introduced as necessitated by amendment.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "control transistor", "variable resistor", and "variable impedance output driver" in a same circuit (claim 27) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7-9, 21, 22, 24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwak et al. (US 2002/0039044).

As to claim 1, Kwak et al. discloses in figure 3 a current reference comprising: a current mirror circuit (140) to force a first current (I2) to be substantially equal to a second current (I1); a control transistor (Q10) coupled to the current mirror circuit to receive the first current, the

control transistor having first and second bias terminals (gate and source) across which a bias voltage can be applied; a variable resistor (Q12) (the impedance of transistor 12 is varied in respond to the control voltage Vrefb. Therefore, transistor 12 is a variable resistor) coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and a control loop (120) responsive to a generated current (current going through Q13) equal to one of the first and second currents (transistor Q13 having the same size with transistor Q8 and Q9, and having the same gate voltage. Therefore, the current going through Q13 is equal to the current going through Q8 and Q9) to influence the biasing voltage.

As to claim 7, figure 3 shows the control transistor (Q10) comprises a NFET, and the first and second biasing terminals are a gate source of the NFET.

As to claim 8, figure 8 shows a second NFET (Q11) having drain terminal coupled to receive the second current from the current mirror, and having a source terminal coupled to provide the second current to the variable resistor.

As to claim 9, figure 3 shows a transistor (Q11) coupled drain-to-source between the current mirror and the variable resistor.

As to claim 21, figure 3 shows a current reference comprising a control transistor (Q10) having a gate terminal and source terminal; a variable resistor (Q12) coupled across the gate terminal and the source terminal of the control transistor, the variable resistor coupled receive a generated current; and control loop circuit (120) responsive to a current equal to the generated current, the control loop circuit coupled to influence the generated current.

As to claim 22, figure 3 shows a current mirror (140) coupled to the control transistor and the variable resistor.

As to claim 24, figure 3 shows the control loop circuit comprises a comparator (Q13) responsive to an output node of the current mirror.

As to claim 26, figure 3 shows a transistor (Q11) coupled to support a variable voltage between the current mirror and the variable resistor.

As to claim 27, figure 3 shows an integrated circuit comprising: a control transistor (Q10) coupled in a first leg of a current reference circuit (140), the control transistor having first and second biasing terminals (gate and source); a variable resistor (Q12) coupled in a second leg of the current reference circuit and between the first and second biasing terminals of the control transistor; and a control loop circuit (120) to modify a resistance value of the variable resistor, the control loop circuit comprising a variable impedance output driver (Kwak et al. teaches that the number of transistors Q14-16 may be varied. Therefore, the impedance of circuit 120 is varied as the number of transistors of Q14-Q16 varied).

Allowable Subject Matter

4. Claims 2-5, 23, 25 and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6 and 10-20 are allowed.

Claims 2-5 and 23 would be and claim 6 is allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a variable resistor, wherein the variable resistor (120) comprises a plurality of resistive devices in parallel or having binary weighted valued.

Claims 10-20 are allowable because the prior art fails to teach or suggest a circuit (such as figure 3) having a control loop circuit (304, 306) having an input node coupled to an output node of the second current reference, and having an output node to influence the first and second variable resistors.

Claims 25 and 28-30 would be allowable because the prior art fails to teach a circuit such as figure 3 having state machine (306).

Response to Arguments

5. Applicant's arguments have been fully considered but they are not persuasive. Applicants argue that "Kwak et al. does not disclose a control loop circuit responsive to a current". The Examiner respectfully disagrees. The gate of Kwak et al.'s Q12 responses a current equal to (Evcc-Vref)/resistance of Q13 to control the current (I), thereby influence the generated current (I1). Applicants further argues that Kwak fails to shows a variable impedance driver. However, Kwak et al. teaches that the number of transistors Q14-16 may be varied. Therefore, the impedance of circuit 120 is varied as the number of transistors of Q14-Q16 varied.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
September 12, 2003

Terry D. Cunningham
Primary Examiner